LED Driver Achieves Electrolytic Capacitor-Less and Flicker-Free Operation With an Energy Buffer Unit

Peng Fang, *Member, IEEE*, Bo Sheng, *Student Member, IEEE*, Samuel Webb, *Student Member, IEEE*, Yan Zhang, *Member, IEEE*, and Yan-Fei Liu, *Fellow, IEEE*

***Abstract*—Electrolytic capacitors are often needed to provide the high-density energy storage required by ac-powered LED drivers; however, they are also well known for their short lifespans. Eliminating electrolytic capacitors in ac–dc LED driver design has become a very important target to improve LED driver technology. In this paper, a cycle-by-cycle energy buffering LED driver has been proposed to achieve electrolytic capacitor-less flicker-free operation. An energy buffering unit, with high-voltage film capacitors being the energy storage device, is introduced in the design to buffer the imbalanced energy in every switching cycle. The switching current can be controlled to meet high power factor correction requirement, while maintaining dc LED output current at the same time. Compared to previous electrolytic capacitor-less designs, this technology can reduce circulating power and, therefore, power conversion loss. A 15-W experimental prototype had been built and tested to verify the proposed LED driving method.**

***Index Terms*—Cycle-by-cycle energy buffering, electrolytic capacitor-less design, flicker-free operation, LED driver.**

I. Introduction

LED lighting has been steadily increasing in popularity, owing largely to its high efficacy, long lifespan, and environment friendly operation. It is replacing fluorescent lighting and becoming the primary artificial lighting sources in many applications. Although having inherent advantages over fluorescent lighting, there are several technical challenges that need to be overcome to fully take advantage of LED lighting, particularly with the ac-powered LED driver. In an ac-connected driver, the notorious double-line-frequency flicker,which can cause numerous health issues, will occur unless the driver is properly designed to eliminate it. Therefore, the key to realizing the full benefits of LED lighting lies in LED driver designs. Also, LED drivers heavily determine the size, efficiency, and cost of LED lighting fixtures, playing a critical role in LED lighting deployment.

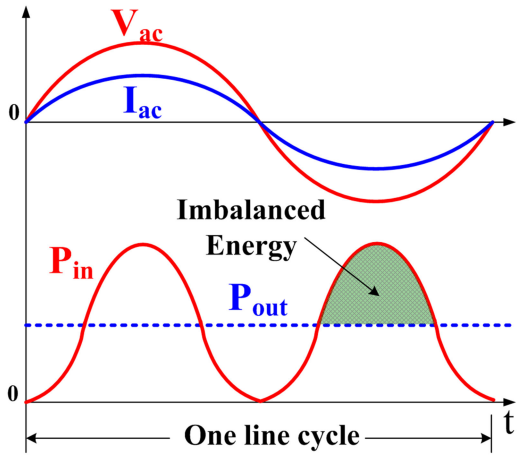

Fig. 1. Energy imbalance between ac input power and expected LED output power with grid-connected LED drivers.

EnergyStar requires power factor correction (PFC) to be implemented for lighting devices higher than 5 W. The power factor must be higher than 0.9 for commercial usages and 0.7 for residential usages [1], which results in a time-varying input power with a double-line-frequency ripple, as shown in Fig. 1. On the other side, achieving flicker-free LED driving requires constant output power. Therefore, energy buffering for double-line-frequency imbalanced energy is required. A conventional single-stage LED driver uses the simplest form of energy buffering, by paralleling bulky electrolytic capacitors at its output. Part of the ripple power is buffered by the storage capacitor, while the remaining escapes to the LED load and, therefore, generates double-line-frequency flicker. Only an infinitely large storage capacitor can buffer 100% of the ripple power using this technique. Thus, double-line-frequency flicker is always present with a single-stage LED-driver-based design. The recommended low-risk flicker level should be less than $0.08 \times f_{\text{flicker}}$ percent of the average [3], which is equivalent to 10% for 120-Hz flicker (under 60-Hz mains) and 8% for 100-Hz flicker (under 50-Hz mains), respectively. Commercially available single-stage LED drivers usually exceed the recommended safe level.

Double-line-frequency flicker raises health-related concerns. Although usually not visible, it can be picked up by retina that leads to visual fatigue and other problems [4], [5]. Conventional

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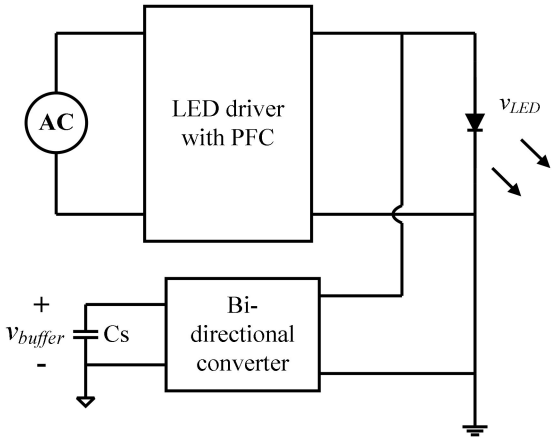

Fig. 2. General implementation of an active filtering LED driver [21].

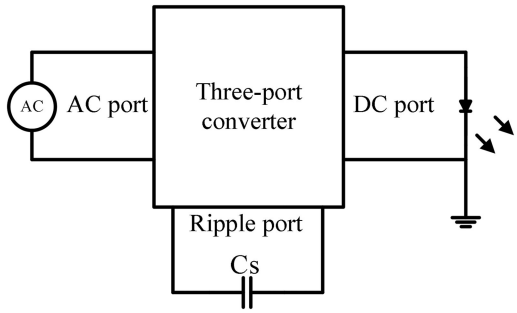

Fig. 3. General implementation of a three-port electrolytic capacitor-free LED driver [23].

two-stage LED drivers can naturally achieve flicker-free LED driving. The additional dc–dc stage in a two-stage design can filter the double-line-frequency ripple power. The drawback is additional loss from the extra power stage and higher cost due to the additional components.

A variety of LED driving methods have been investigated to achieve flicker-free LED driving performance while maintaining high efficiency and low cost. Some focus on novel control strategies, while others focus on power topologies. For instance, the harmonic current injection method had been proposed to reduce imbalanced energy in a half line cycle [6]. Similar methods include input or output current shaping [7]–[9]. They can lessen the severity of flicker, but cannot completely remove it. There are also two-stage integration methods [10]–[12] that share components between the first and the second power stages, leading to a reduction in component count and lower cost. However, optimal operation is difficult to achieve because of extra constraints from component sharing. Ripple cancelation methods [14]–[18] have also been proposed to achieve flicker-free operation. An opposite ripple voltage is produced to cancel the double-line-frequency ripple voltage from the main PFC circuit. A dc LED voltage and LED current can be produced to achieve flicker-free operation. This method can achieve very good efficiency and reduce requirement on storage capacitors. It is possible to achieve electrolytic capacitor-less design, but only for high LED output voltage applications [17].

In addition to eliminating flicker, one other important research area for LED drivers is eliminating electrolytic capacitors. Electrolytic capacitors are often used as high-density energy storage device, buffering the double-line-frequency imbalanced energy. However, it compromises system life. Like other semiconductor devices, LEDs can last for decades. On the other side, the lifespan of electrolytic capacitors is an order of magnitude less [19]. Therefore, eliminating them in LED driver designs becomes paramount.

High-voltage film capacitors have sometimes been used as storage capacitors to replace electrolytic capacitors. By allowing a large double-line-frequency ripple voltage on the high-voltage film capacitor, small capacitors, usually in the range of a few microfarads, can be used. Designs come in different forms under this basic concept. There are active filter methods [20]–[22] that parallel a bidirectional dc–dc converter to an LED load, as shown in Fig. 2. The bidirectional converter serves as an infinite capacitor. When $P_{\rm in} > P_{\rm LED}$, the bidirectional converter transfers extra energy to the film capacitor; when $P_{\rm in} < P_{\rm LED}$, the energy is transferred back to the LED load from the film capacitors. In general, active filter LED drivers generate quite sizeable loss. The half line cycle imbalanced energy, which is around one-third of the total delivered energy, goes through three power convesion steps. First, when $P_{\rm in} > P_{\rm LED}$, the imbalanced energy is transferred from the ac input side to the dc output side. Second, it is then transferred from the dc output side to the storage capacitors. Third, when $P_{\rm in} < P_{\rm LED}$, the energy in the storage capacitor is transferred back to the LED output. Because of excessive power circulation, the projected efficiency is much lower than a conventional single-stage LED driver, and this is evidenced in [21]. Similarly, there are also three-port power decoupling methods [23]–[27] that dedicate a third port for ripple power, as shown in Fig. 3.

A cycle-by-cycle current energy buffering flyback LED driver has been proposed in this paper. It can be considered as an alternative three-port LED driver, but with completely different operating principle. The method treats imbalanced energy at a switching frequency level, resulting in the following benefits.

1) The imbalanced energy experiences one less circulation through the system. When $P_{\rm in} >$ LED, the imbalanced energy is directly transferred from the ac input to the storage capacitors. The imbalanced energy only experiences one power conversion step during this process instead of two times in active filtering and previous three-port LED drivers, which results in a higher efficiency.
2) The maximum energy that needs to be stored in the main flyback transformer, in every switching cycle, is half the amount that of conventional designs and other three-port LED drivers. With the proposed design, the maximum energy that needs to be stored in the flyback transformer is constant in every switching cycle and proportional to the LED output power. On the contrary, with conventional or other electrolytic capacitor-less design, the maximum energy that needs to be stored in the flyback transformer is proportional to the peak input power, which is double the amount of the LED output power. Therefore, a smaller magnetic core can be used for the main flyback transformer, and the current stress for power components is reduced, allowing for lower current rated devices to be used.

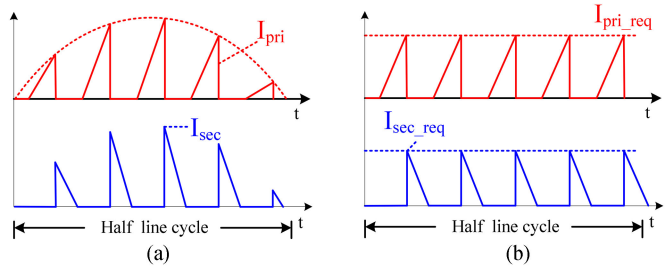

Fig. 4. Primary-side and secondary-side switching current waveforms. (a) Conventional Flyback LED driver with PFC implementation. (b) Expected waveforms to achieve constant LED current output.

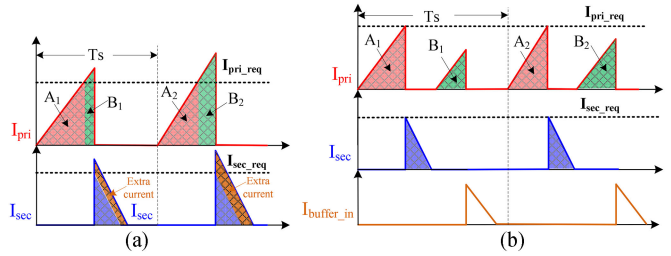

Fig. 5. Illustration of switching current when $P_{\rm in} > P_{\rm LED}$. (a) Conventional design waveforms. (b) Conceptual waveforms achieve energy buffering.

3) Primary-side control can be easily implemented with the proposed LED driver. The signals required to build the LED current regulation loop can be sensed at the primary side. Eliminating the need for a secondary-side control circuit can achieve reduced design complexity and cost.

The remaining part of this paper is organized as follows. Section II presents the design concept and operating principle of the proposed LED driver. Section III discusses the component requirement. The control scheme is discussed in Section IV, and the loss analysis is provided in Section V. The design procedure and consideration are discussed in Section VI. The simulation and experimental results are presented in Section VII. Finally, this paper is concluded in Section VIII.

II. Design Concept and Operating Principle

For a conventional single-stage LED driver, PFC and dc LED output power cannot be achieved at the same time. A flyback LED driver operating under the discontinuous conduction mode (DCM) is used as an example to illustrate this point. Fig. 4(a) shows the primary-side and the secondary-side switching currents, $I_{\rm pri}$ and $I_{\rm sec}$, of a conventional flyback LED driver when PFC is performed. Fig. 4(b) shows the required primary-side and secondary-side switching current that can deliver constant LED output current. As shown, performing PFC requires the peak primary-side switching current to follow the input voltage. On the contrary, delivering constant LED output power requires identical secondary-side switching current in every switching cycle. Therefore, the switching current waveforms need to be changed to bridge the different requirements of these two.

Fig. 5 shows two different patterns of switching current when $P_{\rm in} > P_{\rm LED}$. Fig. 5(a) shows the switching current in a conventional design. When PFC is performed, the peak primary-side switching current is higher than $I_{\rm pri\_req}$, which is the amount required from the LED output. Fig. 5(b) shows the conceptual change on the switching current. The current drawn from the ac input happens in two occasions, and the areas A1 (or A2) and B1 (or B2) are used to represent them. When the primary-side switching current hits $I_{\rm pri\_req}$, the primary-side current is ended as the switch controlling it is turned OFF. The magnetic current commutes to the secondary side, and the extra amount of current is delivered to the LED output. When $I_{\rm sec}$ becomes zero, more primary-side current is drawn from the ac input, as represented by area B1, to meet the requirement from PFC. Area B1 in Fig. 5(b) is equal to area B1 in Fig. 5(a). Therefore, the total current drawn from the ac input depicted in Fig. 5(b) is the same as it is depicted in Fig. 5(a). After the second portion of the primary-side current, the energy stored in the transformer is used to charge another conceptual load instead of feeding the LED output. The remaining energy is represented by the magnetic current, $I_{\rm buffer\_in}$.

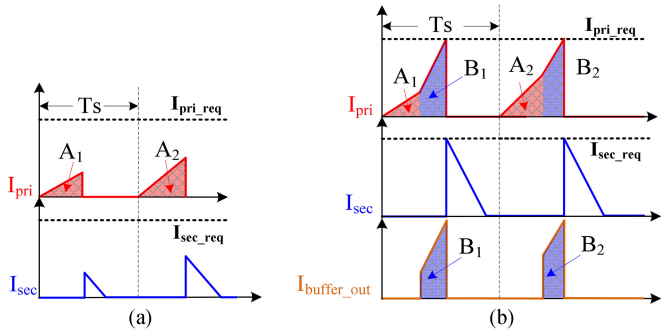

Fig. 6. Illustration of switching current when $P_{\rm in} < P_{\rm LED}$. (a) Conventional design waveforms. (b) Conceptual waveforms achieve energy buffering.

Fig. 6 shows two different patterns of switching current when $P_{\rm in} < P_{\rm LED}$. Fig. 6(a) represents the waveforms in a conventional design. The primary-side switching current is terminated when enough current is drawn from the ac input, as represented by area A1, for PFC. Under this condition, the peak primary-side switching current is still lower than $I_{\rm pri\_req}$, the amount required for constant LED output current. Fig. 6(b) shows a conceptual change on the switching current. After enough current is drawn from the ac input, also represented by area A1, the remaining primary-side switching current is supplied by a conceptual source and is also represented by $I_{\rm buffer\_out}$. As the current drawn from the ac input is the same in both cases, the PFC performance is maintained. The primary-side switching current stops when it hits $I_{\rm pri\_req}$. The extra current supplied by the conceptual source also means extra energy supplied by the conceptual source.

A storage capacitor can serve as the voltage source when $P_{\rm in} < P_{\rm LED}$. It can also serve as the load when $P_{\rm in} > P_{\rm LED}$. Therefore, in every switching cycle, the imbalanced energy is buffered by the energy storage capacitor. To achieve the above current repatterning concept, an interfacing circuit needs to be designed between the storage capacitor and a conventional LED driver, and the proposed LED driver is shown in Fig. 7.

The power stage is based on the flyback topology with an extra energy buffer unit to achieve high power factor and constant

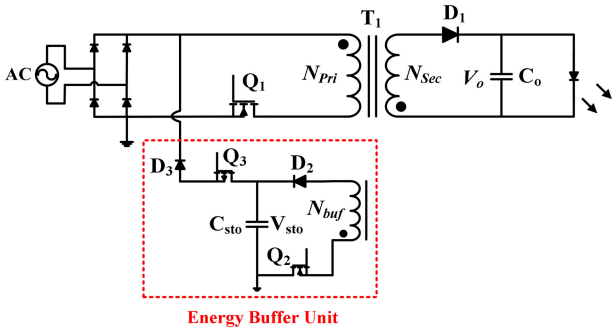

Fig. 7. Proposed cycle-by-cycle energy buffering LED driver.

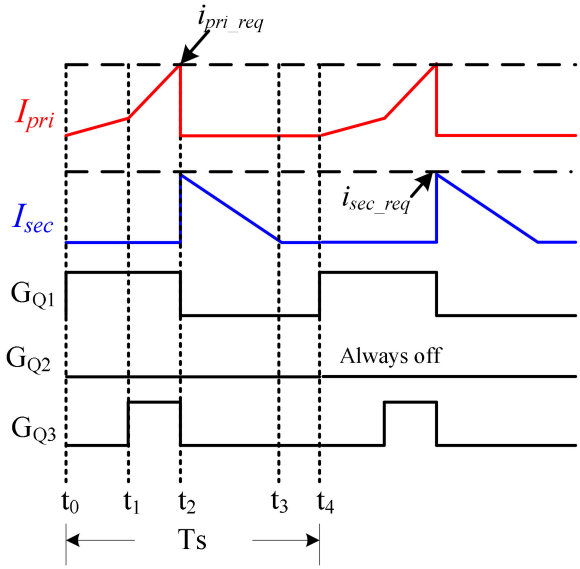

Fig. 8. Key switching waveforms of the proposed LED driver when $P_{\rm in} < P_{\rm LED}$.

current output in every switching cycle. When $P_{\rm in} < P_{\rm LED}$, the additional energy is supplied from the storage capacitor $C_{\rm sto}$ to the LED load. When $P_{\rm in} > P_{\rm LED}$, the extra energy is stored into $C_{\rm sto}$. The output capacitor C_o is implemented by a 10-μF ceramic capacitor in the experimental prototype to filter the switching frequency ripple. The storage capacitor $C_{\rm sto}$ is implemented with a 2 $\times$ 3.3 μF 450-V film capacitor. The switching operations during $P_{\rm in} < P_{\rm LED}$ and $P_{\rm in} > P_{\rm LED}$ are different, and they will be discussed separately.

A. Operation When $P_{\rm in} < P_{\rm LED}$

The LED driver is operated under the DCM with four distinct time intervals $[t_0$–$t_1]$, $[t_1$–$t_2]$, $[t_2$–$t_3]$, and $[t_3$–$t_4]$ in one switching cycle. The critical switching waveforms are shown in Fig. 8.

1) During $[t_0$–$t_1]$: Fig. 9(a) illustrates the circuit operation during the time interval $[t_0$–$t_1]$ when $P_{\rm in} < P_{\rm LED}$. The MOSFET Q_1 is turned ON at t_0 and the current is drawn from the ac input. Because the primary-side winding, $N_{\rm pri}$, is oriented in the flyback mode with respect to the secondary-side windings, $N_{\rm sec}$, and buffer winding, $N_{\rm buf}$, diodes D_1 and D_2 are reverse biased. During this time interval, Q_2 and Q_3 are OFF. The body diode of Q_2 is forward biased. The voltage on D_1 can be expressed as

$$V_{D1\text{-}(P_{\rm in}<P_{\rm LED})}[t_0 - t_1] = V_o + V_{\rm in} \times \frac{N_{\rm pri}}{N_{\rm sec}}. \quad (1)$$

The voltage on diode D_2 can be expressed as

$$V_{D2\text{-}(P_{\rm in}<P_{\rm LED})}[t_0 - t_1] = V_s + V_{\rm in} \times \frac{N_{\rm buf}}{N_{\rm pri}}. \quad (2)$$

The voltage $V_{\rm sto}$ is designed to be higher than $V_{\rm in\_rec}$ when $P_{\rm in} < P_{\rm LED}$. Therefore, diode D_3 is forward biased, and the body diode of Q_3 is reverse biased. The voltage across Q_3 can be expressed as

$$V_{Q3\text{-}(P_{\rm in}<P_{\rm LED})}[t_0 - t_1] = V_{\rm sto} - V_{\rm in\_rec}. \quad (3)$$

This interval ends at time t_1 when the switching current drawn from the ac input reaches the level required for PFC.

2) During $[t_1$–$t_2]$: Fig. 9(b) illustrates the circuit operation during the time interval $[t_1$–$t_2]$. MOSFET Q_3 is turned ON at t_1 and Q_1 is remaining ON. Because $V_{\rm sto}$ is higher than $V_{\rm in\_rec}$, the input bridge rectifier is reversed biased, and there is no more current drawn from the ac input during this time interval. $C_{\rm sto}$ provides the switching current in primary-side winding instead. No ac input current during $[t_1$–$t_2]$ is desirable as enough ac current had been drawn for PFC during $[t_0$–$t_1]$. D_1 and D_2 are still reverse biased, and Q_2 is forward biased. As the voltage on the primary-side winding becomes $V_{\rm sto}$, the voltages on diodes D_1 and D_2 during this time interval also change and become

$$V_{D1\text{-}(P_{\rm in}<P_{\rm LED})}[t_1 - t_2] = V_o + V_s \times \frac{N_{\rm pri}}{N_{\rm sec}} \quad (4)$$

$$V_{D2\text{-}(P_{\rm in}<P_{\rm LED})}[t_1 - t_2] = V_s + V_s \times \frac{N_{\rm buf}}{N_{\rm pri}}. \quad (5)$$

This time interval ends at time t_2 when the primary-side switching current hits $I_{\rm pri\_req}$, which represents the current level required for delivering a constant LED output current. $I_{\rm pri\_req}$ is automatically generated by a feedback loop that will be discussed in Section V. Both Q_1 and Q_3 are turned OFF at t_2.

3) During $[t_2$–$t_3]$: Fig. 9(c) illustrates the circuit operation during the time interval $[t_2$–$t_3]$. As Q_1 and Q_3 are turned OFF at t_2 and Q_2 is still OFF, the magnetic current is forced to commute from the winding $N_{\rm pri}$ to the winding $N_{\rm sec}$. The voltage on the secondary-side winding is clamped at V_o with ignoring the forward voltage drop on D_1. The voltage on the secondary-side winding is reflected to the primary-side winding and the buffer winding. The voltage across the primary-side winding can be expressed as

$$V_{N\rm pri\text{-}(P_{\rm in}<P_{\rm LED})}[t_2 - t_3] = V_o \times \frac{N_{\rm pri}}{N_{\rm sec}}. \quad (6)$$

The voltage on Q_1 can, therefore, be expressed as

$$V_{Q1\text{-}(P_{\rm in}<P_{\rm LED})}[t_2 - t_3] = V_{\rm in\_rec} + V_o \times \frac{N_{\rm pri}}{N_{\rm sec}}. \quad (7)$$

The voltage across winding $N_{\rm buf}$ can be expressed as

$$V_{N\rm buf\text{-}(P_{\rm in}<P_{\rm LED})}[t_2 - t_3] = V_o \times \frac{N_{\rm buf}}{N_{\rm sec}}. \quad (8)$$

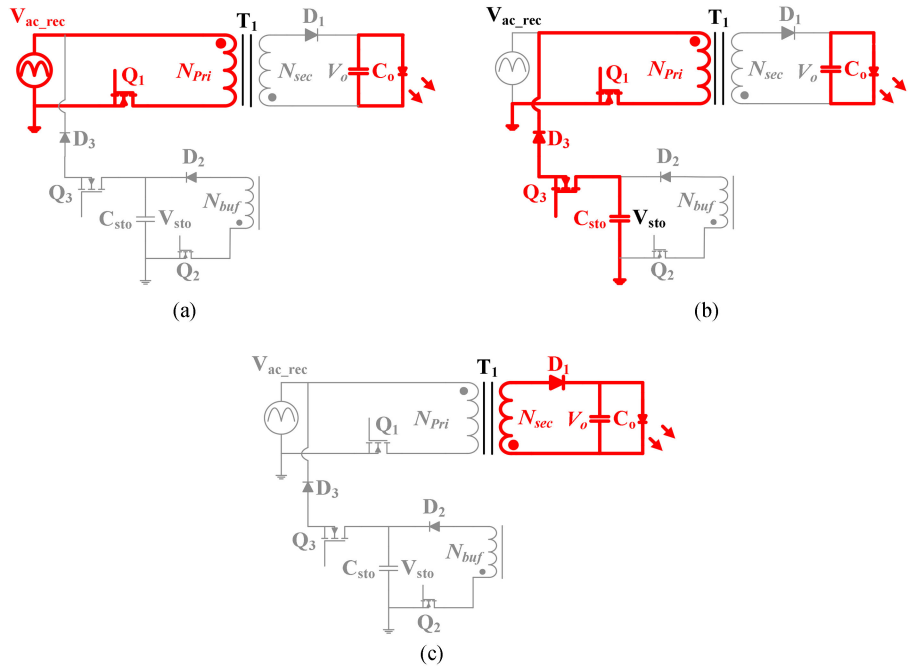

Fig. 9. Switching operation when $P_{\rm in} < P_{\rm LED}$. (a) During $[t_0$–$t_1]$. (b) During $[t_1$–$t_2]$. (c) During $[t_2$–$t_3]$.

In the proposed LED driver, $V_{\rm sto}$ is designed to be always smaller than the voltage on the buffer winding during $[t_2$–$t_3]$ given by (8). Therefore, diode D_2 is forward biased, while the body diode of Q_2 is reverse biased. The voltage on Q_2 can be expressed as

$$V_{Q2\_(P_{\rm in}<P_{\rm LED})}[t_2-t_3] = V_{N{\rm buf}\_(P_{\rm in}<P_{\rm LED})}[t_2-t_3] - V_{\rm sto} = V_o \times \frac{N_{\rm buf}}{N_{\rm Sec}} - V_{\rm sto}. \quad (9)$$

The status of D_3 and Q_3 is the same as it is in the interval $[t_0$–$t_1]$. The magnetic current in winding $N_{\rm sec}$ starts decreasing at t_2 and becomes zero at t_3, which ends this time interval.

4) During $[t_3$–$t_4]$: An idle interval $[t_3$–$t_4]$ is followed to achieve DCM operation. No active switching operation happens in this interval.

B. Operation When $P_{\rm in} > P_{\rm LED}$

When $P_{\rm in} > P_{\rm LED}$, the extra energy is transferred from the ac input to the storage capacitor $C_{\rm sto}$ in every switching cycle. Fig. 10 shows the key switching waveforms with one switching cycle being divided into five time intervals: $[t_0' - t_1']$, $[t_1' - t_2']$, $[t_2' - t_3']$, $[t_3' - t_4']$, and $[t_4' - t_5']$.

1) During $[t_0' - t_1']$: Fig. 11(a) shows the circuit operation during the time interval $[t_0$–$t_1]$ when $P_{\rm in} > P_{\rm LED}$. It is the same as Fig. 9(a) when $P_{\rm in} < P_{\rm LED}$. Therefore, (1) and (2) can be reused to describe voltage stresses of D_1 and D_2. The voltages on Q_3 and D_3 depend on the instantaneous value of $V_{\rm in\_rec}$ and $V_{\rm sto}$. Both $V_{\rm in\_rec}$ and $V_{\rm sto}$ change in a half line cycle, and the situation can change between $V_{\rm in\_rec} > V_{\rm sto}$ and $V_{\rm in\_rec} < V_{\rm sto}$.

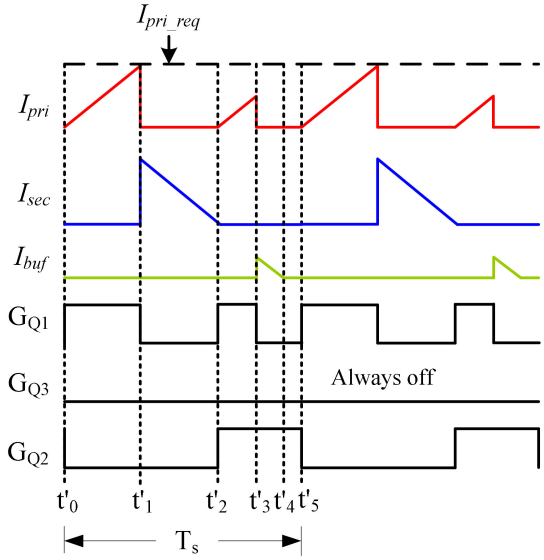

Fig. 10. Key switching waveforms of the proposed LED driver when $P_{\rm in} > P_{\rm LED}$.

The voltage on Q_3 and D_3 can be expressed as

$$V_{D3\_(P_{\rm in}>P_{\rm LED})}[t_0' - t_1'] = \max\{(V_{\rm in\_rec} - V_{\rm sto}), 0\} \quad (10)$$

and

$$V_{D3\_(P_{\rm in}>P_{\rm LED})}[t_0' - t_1'] = \max\{(V_{\rm sto} - V_{\max}), 0\}. \quad (11)$$

As Q_3 is always OFF when $P_{\rm in} < P_{\rm LED}$, the voltage stresses of Q_3 and D_3 remain unchanged in the entire switching cycle. At t_1, the primary-side winding reaches $I_{\rm pri\_req}$ and Q_1 is turned OFF. One should note that the current drawn from the ac input

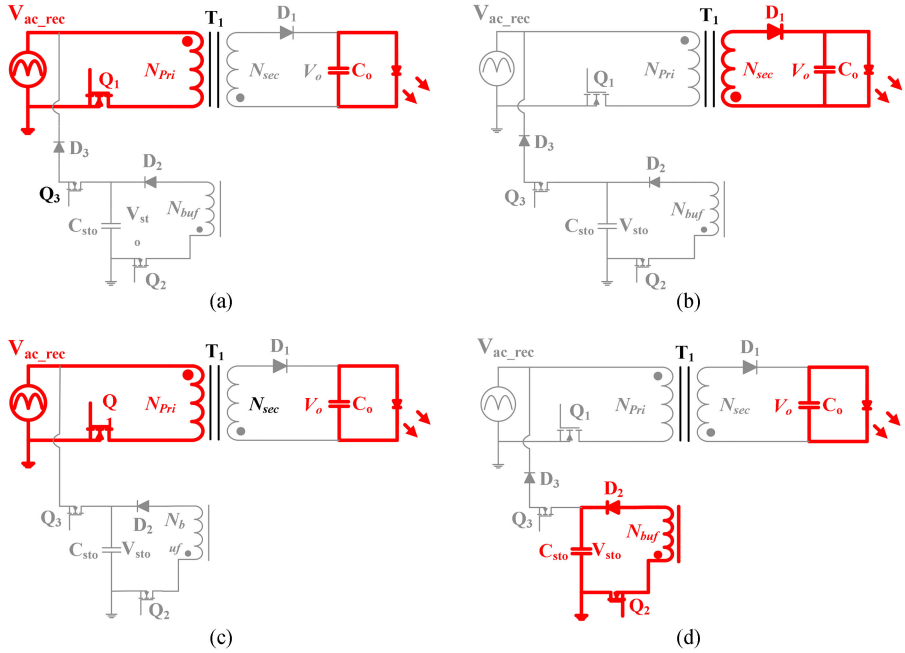

Fig. 11. Switching operation when $P_{\rm in} > P_{\rm LED}$. During $[t_0' - t_1']$. During $[t_1' - t_2']$. During $[t_2' - t_3']$. During $[t_3' - t_4']$.

is not sufficient to perform PFC yet at t_1. More current will be drawn from the ac input during the time interval $[t_2' - t_3']$.

2) During $[t_1' - t_2']$: Fig. 11(b) shows the circuit operation during the time interval $[t_1' - t_2']$ when $P_{\rm in} > P_{\rm LED}$. It is the same as Fig. 9(b). Therefore, (7) and (9) can be reused to describe voltage stress for each component. This interval ends at t_2' when the secondary-side current drops to zero.

3) During $[t_2' - t_3']$: Fig. 11(c) shows the circuit operation during the time interval $[t_2' - t_3']$ when $P_{\rm in} > P_{\rm LED}$. Q_1 is turned ON again at t_2 to draw more current from the ac input. The voltage stresses of the components in $[t_2' - t_3']$ are the same as they are in $[t_0' - t_1']$. This time interval ends at t_3 when the exact amount of current required for PFC is drawn from the ac input.

4) During $[t_3' - t_4']$: Fig. 11(d) shows the circuit operation during the time interval $[t_3' - t_4']$ when $P_{\rm in} > P_{\rm LED}$. Since Q_1 is turned OFF at t_4 and the Q_2 is already ON, the magnetic current commutes from winding $N_{\rm pri}$ to winding $N_{\rm buf}$. The magnetic current does not flow in secondary-side winding because of the following relationship in the design:

$$V_{\rm sto} \times \frac{N_{\rm sec}}{N_{\rm buf}} < V_o. \tag{12}$$

When the magnetic current flows in winding $N_{\rm buf}$, the voltage on the winding is clamped at $V_{\rm sto}$. The term on the left side of the "less than" sign of (12) is equal to the voltage reflected to the secondary-side winding at the time. Therefore, the LED output voltage during $[t_3$–$t_4]$ is higher than the secondary-side winding voltage, and diode D_1 is reverse biased to block current. The voltage across D_1 can be expressed as

$$V_{D1\_(P_{\rm in} > P_{\rm LED})}[t_3 - t_4] = V_o - V_{\rm sto} \times \frac{N_{\rm sec}}{N_{\rm buf}}. \tag{13}$$

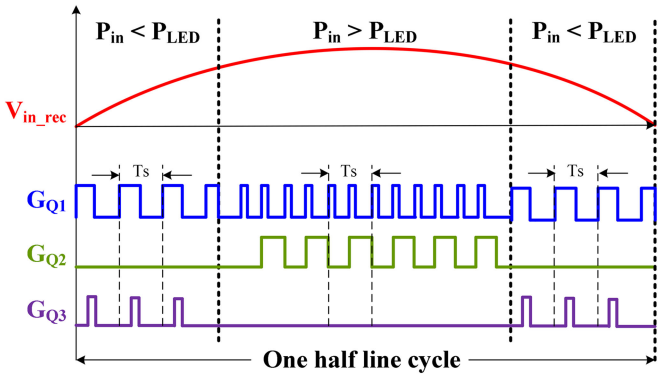

Fig. 12. Switching operation over a half line cycle.

The voltage on the buffer winding is also reflected to the primary-side winding, and the voltage on Q_1 can be expressed as

$$V_{Q1\_(P_{\rm in} > P_{\rm LED})}[t_3 - t_4] = V_{\rm in} + V_{\rm sto} \times \frac{N_{\rm pri}}{N_{\rm buf}}. \tag{14}$$

This time interval ends at t_4 when the magnetic current in winding $N_{\rm buf}$ decreases to zero.

5) During $[t_4' - t_5']$: A small idle time interval $[t_4' - t_5']$ is used to achieve DCM operation. No active switching operation happens in this interval.

C. Overall Operation in a Half Line Cycle

Since the switching operations under both $P_{\rm in} < P_{\rm LED}$ and $P_{\rm in} > P_{\rm LED}$ have been discussed, the overall view of the operation in a half line cycle is illustrated in Fig. 12.

The above discussion also reveals that the imbalanced energy had only gone through two power conversion steps. When $P_{\rm in} > P_{\rm LED}$, the imbalanced energy is transferred from the ac

TABLE I
MAXIMUM VOLTAGE STRESS OF EACH COMPONENT UNDER 110-Vrms INPUT

Q_1	$V_{sto\_max} + V_o \times \frac{N_{pri}}{N_{sec}}$	350V
D_1	$V_{sto\_max} \times \frac{N_{sec}}{N_{pri}} + V_o$	117V
Q_2	$V_o \times \frac{N_{buf}}{N_{sec}} - V_{sto\_min}$	130V
D_2	$\max\left[V_{in\_rec}(t) \times \frac{N_{buf}}{N_{pri}} + V_{sto}(t)\right]$	310V
Q_3	$\max\left[V_{sto}(t) - V_{in\_rec}(t)\right]$	150V
D_3	$\max\left[V_{in\_rec}(t) - V_{sto}(t)\right]$	10V

TABLE II
EXPERIMENTAL PROTOTYPE SPECIFICATION AND KEY COMPONENTS

System Specification	
Input voltage	89 Vrms – 132 Vrms
Maximum output voltage	~60 V
Maximum output current	0.25 A
Maximum output power	15 W
Circuit Parameter	
Transformer	Npri: Nsec: Nbuf = 3:1:3 Lpri=1.2 mH, EE16 core
Switching frequency	25 KHz
Controller	dsPIC33FJ32GS606
MOSFET Q1	STP5N60M2, 600 V, 3.7 A
MOSFET Q2, Q3	FQP3N30, 300 V, 3.2 A
Diode D1, D2, D3	LQA03TC600, 600 V, 3 A
Output capacitor	CGA9N3X7S2A106K230K B, 100 V, 10 μF

input side to the storage capacitor, directly. When $P_{\rm in} < P_{\rm LED}$, it is then transferred from the energy storage capacitor to the LED output side. One less power conversion step is required with the proposed LED driver as compared to an active filter and previous three-port LED drivers.

III. COMPONENT REQUIREMENT ANALYSIS

A. Component Voltage Stress

As the expressions of the component voltage stresses have been derived in each time interval, the maximum voltage stress expression for them in a half line cycle is summarized and shown in Table I. The maximum voltage stresses for them are calculated/simulated in the right column according to the circuit parameters from Table II.

B. Component Current Stress

The switching current in Q_1 peaks at t_2 when $P_{\rm in} < P_{\rm LED}$. It is equal to $I_{\rm pri\_req}$ that is generated by the feedback loop. The switching current in Q_1 peaks two times at t_1 and t_3, respectively, when $P_{\rm in} > P_{\rm LED}$. The peak current at t_1 is also equal to $I_{\rm pri\_req}$, while it is smaller at t_3 except, when $P_{\rm in} = 2P_{\rm LED}$; the peak currents at t_1 and t_3 are equal. Therefore, the maximum current stress of Q_1 in a half line cycle is equal to the $I_{\rm pri\_req}$. There is current in D_3 and Q_3 during $[t_1$–$t_2]$ when $P_{\rm in} < P_{\rm LED}$. The maximum current stress for D_3 and Q_3 is $I_{\rm pri\_req}$ as well. In every switching current, the energy delivered to the LED load, $E_{\rm sec}$, can be expressed as

$$E_{\rm LED} = \frac{1}{2} \times I_{\rm pri\_req}^2 \times L_{\rm pri}. \tag{15}$$

At the same time, $E_{\rm LED}$ can also be expressed as

$$E_{\rm LED} = I_{\rm LED} \times V_o \times T_s. \tag{16}$$

Combining (15) and (16) yields

$$I_{\rm pri\_req} = \sqrt{\frac{2 \times P_{\rm LED} \times T_s}{L_{\rm pri}}}. \tag{17}$$

Equation (17) describes the relationship between $I_{\rm pri\_req}$ and $I_{\rm LED}$. Once the circuit parameters, $I_{\rm LED}$, V_o, T_s, and $L_{\rm pri}$ are determined, $I_{\rm pri\_req}$ can be calculated. $I_{\rm pri\_req}$ is calculated to be 1 A at the 15-W output power with the circuit parameter from Table II. The maximum current stress with D_1 can be expressed as

$$I_{D1\_\max} = I_{\rm sec\_pk} = I_{\rm pri\_req} \times \frac{N_{\rm pri}}{N_{\rm sec}}. \tag{18}$$

The maximum current of D_1 is calculated to be 3 A. The maximum current in D_2 and Q_2 occurs when $P_{\rm in} = 2P_{\rm LED}$. Under this situation, the primary-side current at t_3 is equal to $I_{\rm pri\_eq}$ as well. Therefore

$$I_{D2\_\max} = I_{Q2\_\max} = I_{\rm LED\_req\_pri} \times \frac{N_{\rm pri}}{N_{\rm buf}}. \tag{19}$$

The maximum current with D_2 and Q_2 is calculated to be 1 A.

It is worth mentioning again that the proposed LED driver allows the use of a smaller core for the transformer and low current rating components. In every switching cycle, the peak secondary-side current is the same and corresponds to a constant output power, $P_{\rm LED}$. In a conventional design or previous active filtering LED drivers, the maximum power delivered to the secondary side is equal to $2P_{\rm LED}$. Therefore, the maximum energy that must be stored in the transformer in the proposed design is only half the amount of these previous designs, which permits using a smaller transformer core and low current rating components.

C. Storage Capacitor Requirement

The high-voltage film capacitor $C_{\rm sto}$ is used to buffer the imbalanced energy in a half line cycle. The value of $C_{\rm sto}$ is determined by the amount of imbalanced energy and the designed voltage range for $V_{\rm sto}$. The relationship among the imbalanced energy, $E_{\rm buffer}$, the minimum voltage of $V_{\rm sto}$, and the maximum voltage of $V_{\rm sto}$ can be expressed as

$$\begin{aligned} E_{\rm buffer} &= \frac{1}{2} C_{\rm sto} \times (V_{\rm sto\_max}^2 - V_{\rm sto\_min}^2) \\ &= C_{\rm sto} \times V_{\rm sto\_avg} \times V_{\rm sto\_pp\_rip} \end{aligned} \tag{20}$$

where

$$V_{\rm sto\_avg} = \frac{V_{\rm sto\_max} + V_{\rm sto\_min}}{2} \tag{21}$$

TABLE III
STORAGE CAPACITOR REQUIREMENT COMPARISON BETWEEN DIFFERENT LED DRIVING SOLUTIONS

Topology	Storage Capacitor Requirement
Single-stage Flyback LED driver	**Voltage rating**: can be decided based on the LED voltage **Capacitance**: High. Determined by the requirement of flicker level. Electrolytic capacitors are required to implement the storage capacitor. Example: 1mF electrolytic capacitors are used on a 12W, 41V LED driver [30]. The normalized capacitance per wattage is 83uF/W.
Two-stage Flyback + Buck LED driver	**Voltage rating**: can be decided based on LED voltage. The Bus voltage is usually designed to be the LED voltage plus a reasonable voltage margin for proper Buck converter operation. For example, 63V voltage rated capacitors can be used when the maximum LED voltage is 50V. **Capacitance**: High. Determined by the acceptable Bus voltage ripple. Usually implemented by electrolytic capacitors. Example: 1mF, 63V, electrolytic capacitors are used in a 30W, 45V, two-stage LED driver design [31]. The normalized capacitance per wattage is 33uF/W.
Proposed cycle by cycle energy buffering LED driver	**Voltage rating**: High. The storage capacitors are biased at high voltage (usually 100V to 300V voltage) and allow a high peak to peak double line frequency voltage ripple. The voltage rating of the storage capacitor is not linked to the LED voltage. **Capacitance**: Low. A few microfarads to enable film capacitor implementation. Eq.(25) can be used to calculate the required capacitor. Example: 2 x 3.3μF, 300V film capacitors are used in the proposed LED driver. The normalized capacitance per wattage is 0.44uF/W in the proposed design.
Previous active filter LED driver	The rule to select the storage capacitor is the same as the proposed LED driver.

and

$$V_{\text{sto\_pp\_rip}} = V_{\text{sto\_max}} - V_{\text{sto\_min}}. \tag{22}$$

$V_{\text{sto\_avg}}$ represents the average voltage of V_{sto} and $V_{\text{sto\_pp\_rip}}$ represents the double-line-frequency peak-to-peak ripple voltage of V_{sto}. Rearranging (22) yields

$$C_{\text{sto}} = \frac{E_{\text{imbalance}}}{V_{\text{sto\_avg}} \times V_{\text{sto\_pp\_rip}}}. \tag{23}$$

At the same time, E_{buffer} can also be expressed as

$$E_{\text{buffer}} = \frac{1}{\pi} P_{\text{LED}} \times \frac{1}{2} \times T_{\text{line}}. \tag{24}$$

Combining (23) and (24) yields

$$C_{\text{sto}} = \frac{P_{\text{LED}} \times T_{\text{line}}}{2\pi \times V_{\text{sto\_avg}} \times V_{\text{sto\_pp\_rip}}}. \tag{25}$$

Equation (25) reveals that the capacitance of C_{sto} is reversely proportional to the average voltage $V_{\text{sto\_avg}}$ and the peak-to-peak ripple amplitude $V_{\text{sto\_pp\_rip}}$. When a higher average voltage $V_{\text{sto\_avg}}$ and/or a larger ripple amplitude $V_{\text{sto\_pp\_rip}}$ are designed in the proposed LED driver, C_{sto} can be reduced to achieve electrolytic capacitor-free design. The energy storage capacitor requirement of the proposed LED driver will be compared to the requirement of other LED driving technologies, and the result is summarized in Table III.

IV. CONTROL STRATEGY

Fig. 13(a) shows the control diagram of the proposed energy buffering LED driver, and Fig. 13(b) and (c) gives the example gate driving logic for both $P_{\text{in}} > P_{\text{LED}}$ and $P_{\text{in}} < P_{\text{LED}}$. There are two control loops, LED current loop and V_{sto} voltage loop, in the system.

In the LED current loop, the LED current is sensed and compared with the reference, $I_{\text{LED\_ref}}$. The compensated error $I_{\text{pri\_req}}$ becomes the boundary of the primary-side switching current. The sensed primary-side switching current $I_{\text{pri\_sns}}$ is compared with $I_{\text{pri\_req}}$. Once $I_{\text{pri\_sns}}$ hits $I_{\text{pri\_req}}$, no more current will be drawn from the primary side. Thus, the peak secondary-side switching current is the same in every switching cycle to achieve constant LED output current. The current feedback loop determines the peak primary (also secondary) side current to achieve LED current regulation.

In the V_{sto} voltage loop, the averaged voltage of V_{sto}, $V_{\text{sto\_avg}}$, is compared with its reference, $V_{\text{sto\_ref}}$. The compensated error V_{s_comp} multiples the scaled input voltage $V_{\text{in\_rec\_}s}$, and the result becomes the reference of the ac input current. The average input current is obtained by taking $I_{\text{pri\_sns}}$ for integration in every switching cycle. The result, $I_{\text{in\_avg}}$, is compared with $I_{\text{in\_ref}}$. Once $I_{\text{in\_avg}}$ hits $I_{\text{in\_ref}}$, no more current will be drawn from the ac input. Therefore, PFC is achieved. The voltage feedback loop determines the ac input current to achieve $V_{\text{sto\_avg}}$ regulation.

Fig. 13(b) illustrates the corresponding gate driving signal when $P_{\text{in}} > P_{\text{LED}}$. At time t_0, Q_1 is turned ON. $I_{\text{in\_avg}}$ is the integrated result of $I_{\text{pri\_sns}}$. $I_{\text{pri\_sns}}$ hits $I_{\text{pri\_req}}$ at time t_1, while

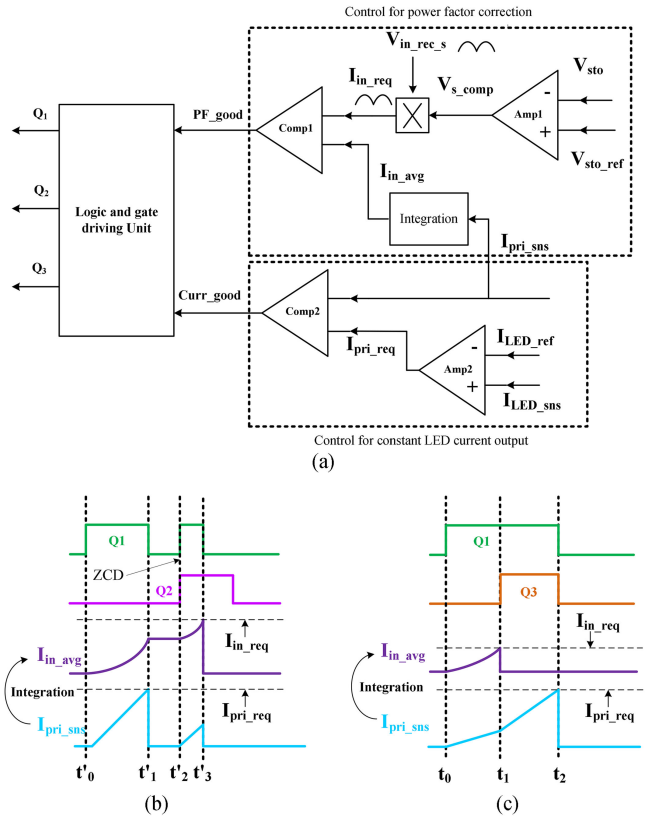

Fig. 13. Control scheme of the proposed LED driver. (a) Control diagram. (b) Gate driving logic when $P_{\rm in} < P_{\rm LED}$. (c) Gate driving logic when $P_{\rm in} > P_{\rm LED}$. (d) Operation flow of the proposed LED driver in a switching cycle.

$I_{\rm in\_avg}$ is still lower than $I_{\rm in\_ref}$. The control system identifies $P_{\rm in} > P_{\rm LED}$. Q_1 is turned OFF at time t_1, and the magnetic current commutes from the primary side to the secondary side. At time t_2, the secondary-side current drops to zero and generates a signal zero current detection (ZCD). During $[t_1$–$t_2]$, $I_{\rm in\_avg}$ is constant as there is no current from the ac input. Q_1 is turned ON again at t_2 and $I_{\rm pri\_sns}$ starts rising from zero. Q_2 is also turned ON at t_2. $I_{\rm in\_avg}$ continues increasing until t_3, when $I_{\rm in\_avg}$ hits $I_{\rm in\_ref}$. Q_1 is turned OFF at t_3, while Q_2 remains ON. The magnetic current commutes from the primary side to the auxiliary side.

Fig. 13(c) illustrates the corresponding gate driving signals when $P_{\rm in} < P_{\rm LED}$. At time t_0, Q_1 is turned ON. $I_{\rm in\_avg}$ is the integrated result of $I_{\rm pri\_sns}$. $I_{\rm in\_avg}$ hits $I_{\rm in\_ref}$ at t_1, while $I_{\rm pri\_sns}$ is still lower than $I_{\rm pri\_req}$. The control system identifies $P_{\rm in} < P_{\rm LED}$. Therefore, Q_3 is turned ON at t_2, and no more current will be drawn from the ac input. The primary-side switching current keeps increasing until t_3, when $I_{\rm pri\_sns}$ hits $I_{\rm pri\_req}$. Both Q_1 and Q_3 are turned OFF then, and the switching current commutes to the secondary side.

It is worth mentioning that the proposed LED driving method enables primary-side current regulation. Under the steady state, the peak secondary-side current in every switching cycle is described by (18). The secondary-side current conduction time, which corresponds to $(t_2$–$t_1)$ in Fig. 8 and $(t_3' - t_2')$ in Fig. 10, can be sensed by detecting winding voltages. Therefore, the averaged secondary-side current in one switching cycle can be

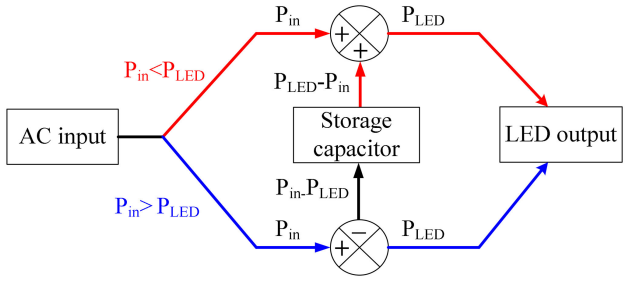

Fig. 14. Power flow of the proposed cycle-by-cycle energy buffering LED driver.

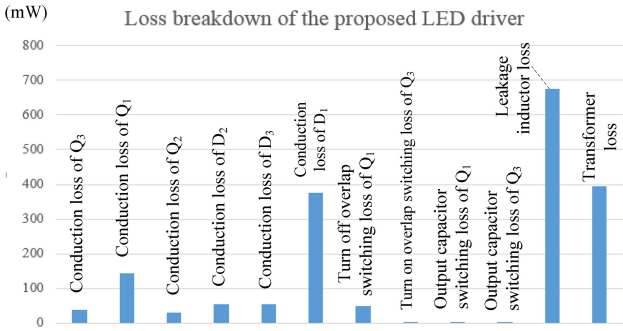

Fig. 15. Loss breakdown of the proposed cycle-by-cycle energy buffering LED driver.

expressed as

$$I_{\rm LED} = \frac{I_{\rm sec\_pk} \times T_{\rm dis}}{2 \times T_s} \tag{26}$$

where $T_{\rm dis}$ is equal to $(t_2$–$t_1)$ in Fig. 8 and $(t_3' - t_2')$ in Fig. 10. Combining (18) and (26) yields

$$I_{\rm LED} = \frac{I_{\rm LED\_req\_pri} \times T_{\rm dis} \times N_{\rm pri}}{2 \times T_s \times N_{\rm sec}}. \tag{27}$$

Once $I_{\rm pri\_req}$ and $T_{\rm dis}$ are available, the LED current can be estimated without additional sensing on the secondary side. Papers [28] and [29] have the details of primary-side circuit sensing technology and will not be further discussed in this paper.

Fig. 14 illustrates the high-level power flow of the proposed cycle-by-cycle energy buffering LED driver. When $P_{\rm in} < P_{\rm LED}$, the storage capacitor will supply the amount of power, $P_{\rm LED} - P_{\rm in}$, to the LED load. When $P_{\rm in} > P_{\rm LED}$, the extra power from the ac input, $P_{\rm in} - P_{\rm LED}$, will be directed to be stored in the storage capacitor.

V. Loss Analysis

In this section, a loss analysis of the proposed cycle-by-cycle energy buffering LED driver, as well as the previous active filtering LED driver, will be performed. To fairly compare the losses from both designs, the parameters of MOSFETs and diodes used in the analysis are standardized. In this way, the analysis has a much less dependence on the component parameter, and the result can strongly reflect the advantages/disadvantages of each design from the perspective of power circuit topology and

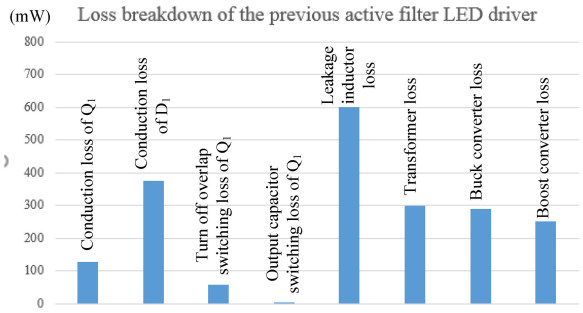

Fig. 16. Loss breakdown of the previous active filtering LED driver.

operation condition. For the proposed cycle-by-cycle energy buffering LED driver, the following losses had been identified.

For MOSFET Q1, under both $P_{\rm in} < P_{\rm LED}$ and $P_{\rm in} > P_{\rm LED}$ operating conditions, there are conduction loss during $[t_0$–$t_1]$, output capacitor switching loss at t_0. When $P_{\rm in} < P_{\rm LED}$, there is turn-OFF overlap switching loss at t_2. When $P_{\rm in} > P_{\rm LED}$, there is turn-OFF overlap switching loss at t_1 and t_3.

For MOSFET Q_2, there is only conduction loss during $[t_3$–$t_4]$ when $P_{\rm in} > P_{\rm LED}$. One should note that the body diode of Q_2 is forward biased before it is turned ON. Therefore, there is no turn-ON overlap switching loss and output capacitor switching loss. There is no turn-OFF switching loss with Q_2 as well, since the switching current in it is already zero before Q_2 is turned OFF.

For MOSFET Q_3, there is turn-ON overlap switching loss and output capacitor switching loss at t_1 when $P_{\rm in} < P_{\rm LED}$. There is no turn-OFF switching loss with Q_3, since its switching current is already zero before Q_3 is turned OFF (turn OFF Q_1 at t_2 terminates the switching current).

For diode D_1, there are conduction losses during $[t_2$–$t_3]$ when $P_{\rm in} < P_{\rm LED}$ and during $[t_1$–$t_2]$ when $P_{\rm in} > P_{\rm LED}$. For diode D_2, there is conduction loss during $[t_3$–$t_4]$ when $P_{\rm in} > P_{\rm LED}$. For diode D_3, there is conduction loss during $[t_1$–$t_2]$ when $P_{\rm in} < P_{\rm LED}$.

There are also losses from the equivalent lump leakage inductance at the primary side. The leakage inductance, between the primary-side main winding and the secondary-side main winding, is estimated to be 4% of the primary-side main winding inductance, due to relatively poor coupling caused by galvanic isolation. The leakage inductance, between the primary-side main winding and the buffering winding, is estimated to be 2% of the primary-side main winding inductance, as galvanic isolation is not required and good coupling can be achieved. When $P_{\rm in} < P_{\rm LED}$, there is energy built up in the leakage inductor as the primary-side switching current grows during $[t_0$–$t_1]$. When $P_{\rm in} > P_{\rm LED}$, there is energy built up in the leakage inductor as the primary-side switching grows during $[t_0$–$t_1]$ and $[t_2$–$t_3]$, respectively. These energies are dissipated in a snubber circuit as loss.

For the flyback transformer, there is core and copper loss. A detailed estimation of this loss requires very complex analysis; however, with a reasonably good design, the total loss from the transformer is estimated to be 2% of the power it will handle.

The detailed loss breakdown of the proposed cycle-by-cycle energy buffering LED driver is shown in Table IV in the Appendix as well as presented in the bar chart in Fig. 15.

Also, the detailed loss breakdown for the previous active filter LED driver is performed, and the result is shown in Table V as well as the bar chart in Fig. 16.

To estimate the power losses from the buck (release imbalanced energy) and boost (store imbalanced energy) converters in the previous active filtering LED driver, the following assumptions are made.

1) The switching frequency of the buck and boost converters is also 25 kHz, which benchmarks the switching frequency of the proposed LED driver.
2) The inductor used in the buck and boost converters is 1.2 mH, which is equal to the inductance value of the primary-side winding of the flyback transformer in the proposed LED driver. In this way, the magnetic components used in both designs are at a comparable level and can be assumed to have the same level of power loss.

The total loss generated by the proposed cycle-by-cycle energy buffering LED driver and the previous active filtering LED driver is calculated/estimated to be 1815 and 2006 mW, respectively, for the 15-W output power. It should be noted that the majority of losses, in both designs, are from diode conduction loss, leakage inductance loss, and transformer loss. Because of low-frequency (25-kHz) operation, the related switching loss is not significant. In addition to the quantitive analysis on the loss breakdown, the loss difference between these two designs can also be understood from the perspective of energy process steps. The proposed LED driver requires one less power conversion step with the imbalanced energy.

Although there are several additional components in the proposed LED driver as compared to a standard single-stage and two-stage LED driver, some of them do not add too much to the overall loss and even help reduce loss. For example, when $P_{\rm in} > P_{\rm LED}$, the imbalanced energy is transferred from the ac input to the storage capacitor. Compared to a standard flyback converter including a MOSFET, a diode and a flyback transformer, there is an additional MOSFET Q_2 involved in the energy transfer in the proposed design. However, there is only conduction loss with Q_2, and the calculated loss is only 30 mW, which is equal to roughly 0.2% of the total output power. On the contrary, the imbalanced energy needs to go through a complete boost power conversion process in the previous active filter LED drivers to complete energy storage. One more power conversion step means more diode conduction loss and inductor loss, which contributes significantly to the total loss. The loss saved with the proposed LED driver, over the previous active filtering LED driver, is around 190 mW, which is equivalent to $\sim$1.2% higher efficiency for 15-W output power designs.

VI. Design Procedures and Considerations

In this section, an example design procedure is provided as a design guideline. Design considerations on switching frequency, transformer inductance, turn ratio, and storage capacitors selection are included.

1) Determine the switching frequency. For example, the switching frequency is designed to be 25 kHz for the experimental prototype to minimize switching loss.
2) Select the turn ratio $N_{\rm pri}$:$N_{\rm sec}$:$N_{\rm buf}$. The turn's ratio determines the voltage stresses of the components. For example, $N_{\rm pri}$:$N_{\rm sec}$:$N_{\rm buf}$ is designed to be 3:1:3 in the experimental prototype.
3) Determine the inductance of the primary-side winding. $L_{\rm pri}$ should be selected to meet the requirement of DCM operation, while, at the same time, minimize idle time in one switching cycle to achieve lowest possible current stresses. In the experimental prototype, $I_{\rm pri}$ is designed to be 1.2 mH.
4) Select the capacitor $C_{\rm sto}$ and the voltage range for $V_{\rm sto}$. With $P_{\rm LED}$ = 15 W, $V_{\rm sto\_avg}$ is chosen to be 140 V and $V_{\rm sto\_pp\_rip}$ to be 60 V, and the required capacitor $C_{\rm sto}$ is calculated to be 5.7 μF with (27). Two 3.3-μF film capacitors are used in the experimental prototype. On the other side, one should note that the voltage stresses of other components are also related to $V_{\rm sto}$, as shown in Table I. Therefore, the voltage range for $V_{\rm sto}$ should be properly selected.
5) Select the output capacitors. Because constant output current is delivered to the output in every switching cycle, the output capacitor C_o is only responsible for filtering the switching frequency ripple. Therefore, small capacitance ceramic capacitors can be selected for the design. A 10-μF 100-V ceramic capacitor is used in the experimental prototype.
6) Calculate the voltage and current stresses of each power semiconductor components and select parts accordingly.

The above steps provide an example procedure to design the proposed LED driver. Like any other designs, it can always start the design procedure in a different order. For example, one can set the maximum voltage stresses and current stresses of components in the beginning and then design other parameters that around this objective.

VII. Simulation and Experimental Result

To verify the operating principle of the proposed LED driver, a 15-W simulation model and experimental prototype had been built, simulated, and tested. The circuit parameter is shown in Table II.

Fig. 17 shows the simulated and measured primary-side switching current waveforms. A rather flat peak primary-side switching current is shown in the simulated result, which completely agrees with the analysis. Due to sensing circuit limitation and delay, the measured primary-side peak switching current has a small level of variation in the measured waveform. Also, because of noise, mis-triggers occur and results in several spikes and dips scattered in a half line cycle period.

Fig. 18 shows the simulated secondary-side switching current and the LED current at line-frequency time scale. The peak secondary-side switching current is a constant in a half line cycle. Therefore, the averaged secondary-side current, which is also equal to the LED current, is a constant in a half line cycle, and flicker-free LED driving performance is achieved.

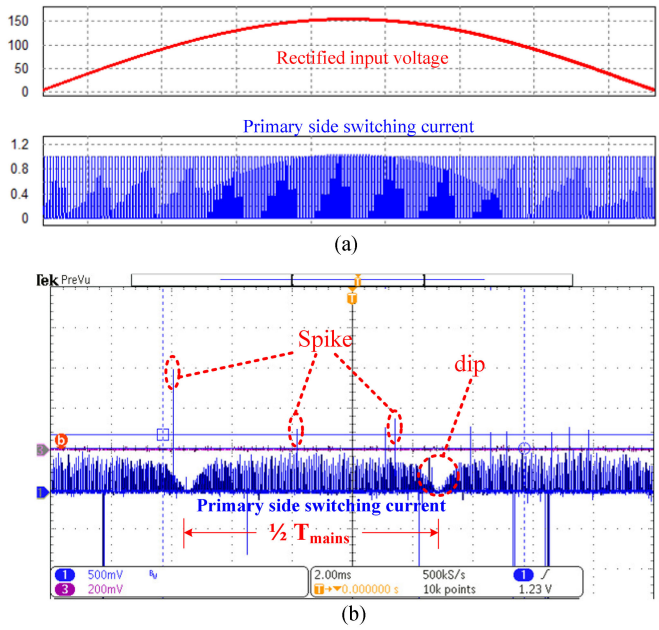

Fig. 17. Primary-side switching current. (a) Simulated result. (b) Measured waveform.

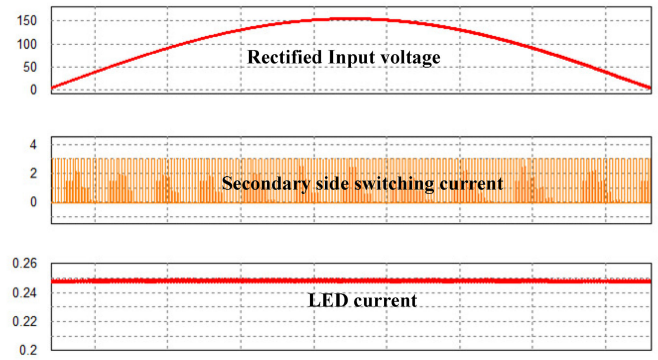

Fig. 18. Simulated key waveforms at line cycle time scale.

Fig. 19 shows the key switching waveforms when $P_{\rm in} < P_{\rm LED}$. The MOSFET Q_1 is turned ON at the beginning of a switching cycle. During [t_0–t_1], the switching current in the Q_1 is drawn from the ac input. At time t_1, enough current is drawn from the ac input required by performing PFC. The MOSFET Q_3 is turned ON at t_1. During [t_1–t_2], the switching current in Q_1 is drawn from the storage capacitor $C_{\rm sto}$. Therefore, energy is transferred from $C_{\rm sto}$ to the transformer and eventually to the LED output after the primary-side switching current is terminated. MOSFET Q_2 is always OFF during this operating condition. The measured waveforms are shown in Fig. 20 and agree with simulated waveforms (the switching current is sensed by resistor and presented in voltage form).

Fig. 21 shows the simulated key switching waveforms when $P_{\rm in} > P_{\rm LED}$. MOSFET Q_1 is turned ON during [t_0–t_1] and the primary-side current in Q_1 is drawn from the ac input. At t_1,

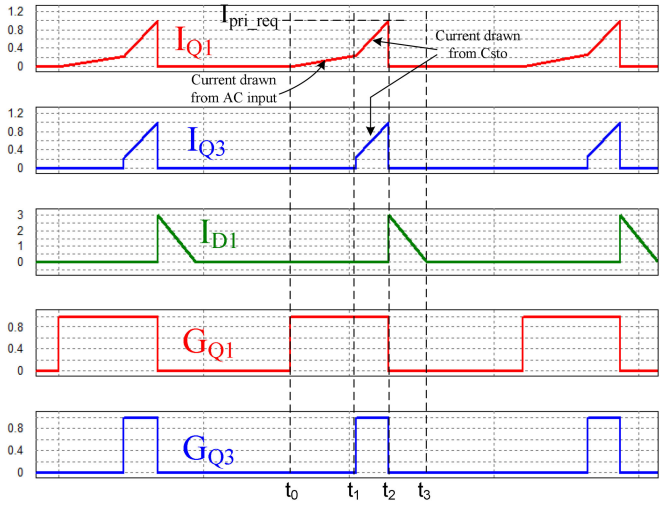

Fig. 19. Simulated key switching waveforms when $P_{\text{in}} < P_{\text{LED}}$.

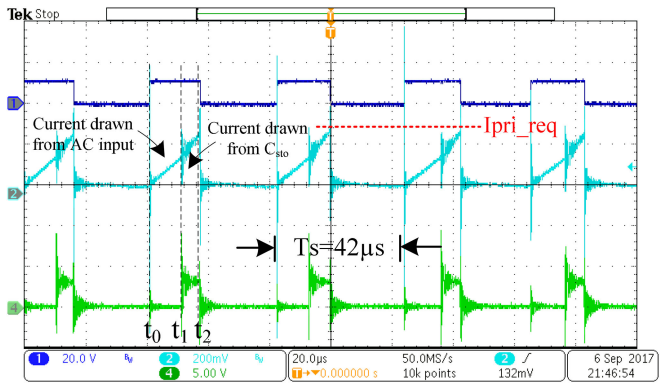

Fig. 20. Key switching waveforms when $P_{\text{in}} < P_{\text{LED}}$.

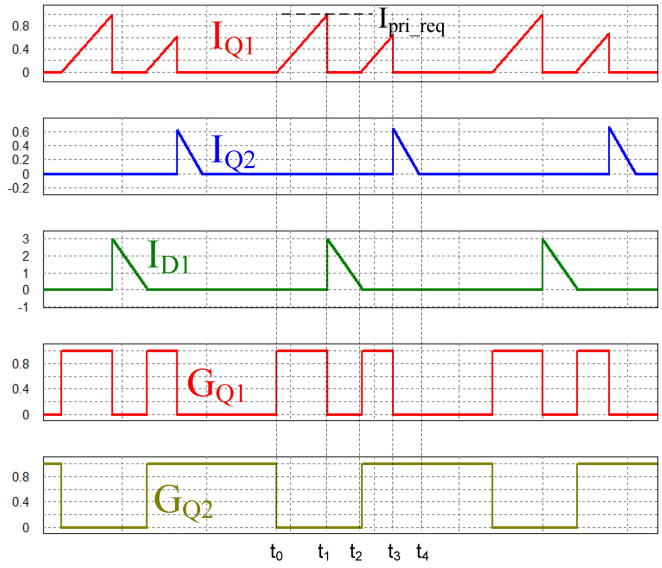

Fig. 21. Simulated key switching waveforms when $P_{\text{in}} > P_{\text{LED}}$.

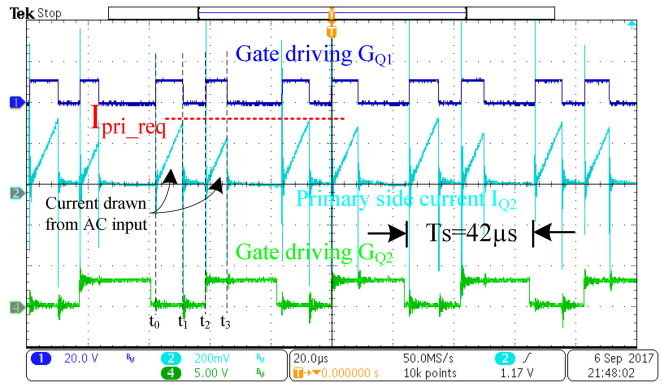

Fig. 22. Key switching waveforms when $P_{\text{in}} > P_{\text{LED}}$.

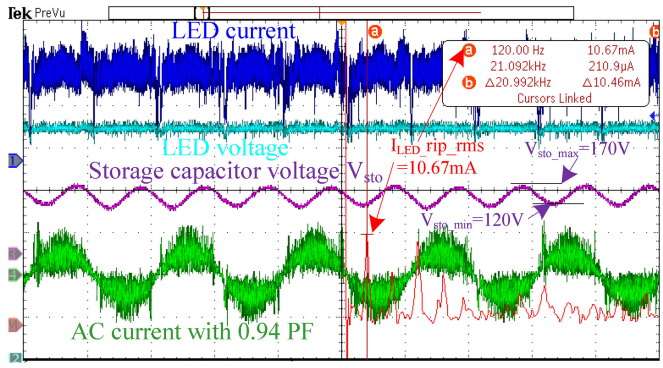

Fig. 23. Key waveforms in double-line-frequency operation.

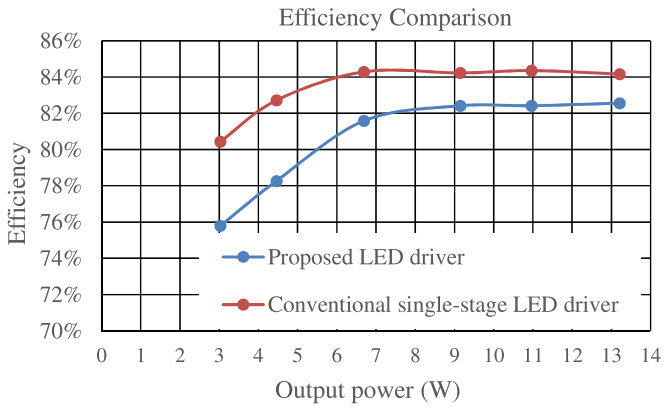

Fig. 24. Efficiency comparison between the proposed LED driver and a conventional LED driver under 110-Vrms input.

the primary-side switching current hits $I_{\text{pri\_req}}$, the level required by the LED output. Q_1 is turned OFF to end the primary-side switching current, and the magnetic current commutes to the secondary-side winding. During $[t_1$–$t_2]$, the magnetic current flows in the secondary-side winding and delivered to the LED load. The secondary-side current drops to zero at t_2 and Q_1 is turned ON again. MOSFET Q_2 is also turned ON at t_2. During $[t_2$–$t_3]$, more current is drawn from the ac input. At t_3, the total current drawn from the ac input reaches the level required by performing PFC and Q_1 is turned OFF again. The magnetic

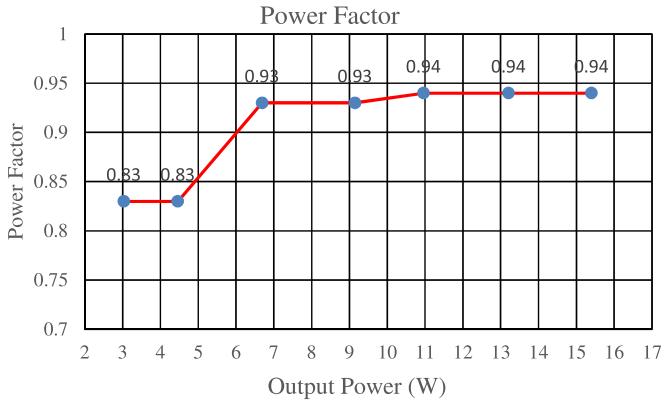

Fig. 25. Power factor performance under 110-Vrms input, full load.

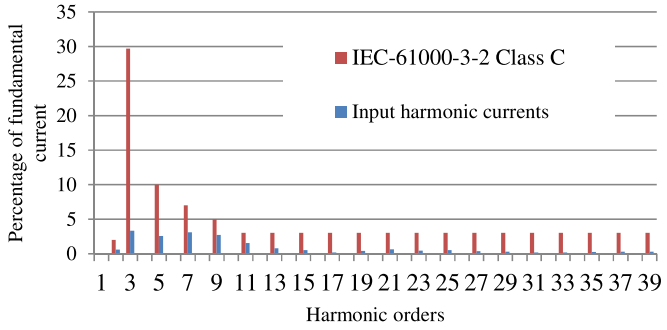

Fig. 26. Input harmonic currents versus IEC-61000-3-2 limit under 110-Vrms input, full load.

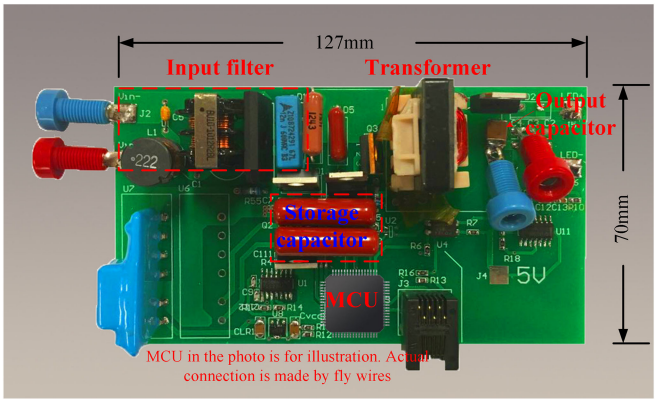

Fig. 27. Photo of the experimental prototype.

current commutes from the primary-side winding to the buffer winding. The extra energy in the transformer is then transferred to the capacitor C_{sto}. MOSFET Q_3 is always OFF during this operation condition. Fig. 22 shows the measured waveforms, and it highly agrees with simulated result.

Fig. 23 shows the key waveforms of line-frequency operation, which includes the ac input current, the LED voltage, the LED current, and the storage capacitor voltage V_{sto}. The LED voltage is almost a constant. The fast Fourier transform function is used to measure 120-Hz ripple LED current to avoid misreading due to switching noise. The RMS ripple LED current at 120 Hz is 10.67 mA, which corresponds to 15-mA peak ripple and is 6% of the average LED current. The voltage on the storage capacitor, V_{sto}, changes from 120 V as the minimum to 170 V as the maximum in a half line cycle, to buffer the imbalanced energy. It is worth mentioning that, due to sensing circuit limitation, the peak of the switching current I_{pri} varies a bit in a half line cycle, which results in a less than ideal output current waveform. A better output current waveform can be achieved with an improved sensing circuit design; the simulation waveform in Fig. 18 verifies that.

Fig. 24 compares the efficiency of the proposed LED driver and a comparable conventional single-stage LED driver. At full load, the efficiency of the proposed LED driver is 1.9% lower than the efficiency of a conventional flyback LED driver, which is a very small price to pay when flicker-free and electrolytic capacitor-free operation have been achieved.

Fig. 25 shows the power factor of the proposed LED driver. At full load, the experimental prototype achieves a power factor of 0.94, which meets the requirement from EnergyStar.

Fig. 26 shows the measurement of input harmonic currents. All harmonic currents of interest are below the limits from IEC-61000-3-2. The photo of the experimental prototype is shown in Fig. 27.

VIII. Conclusion

Eliminating electrolytic capacitors in LED driver designs is critical to extending the lifetime of LED lighting fixtures. An alternative three-port LED driver—cycle-by-cycle energy buffering LED driver—has been proposed in this paper to achieve electrolytic-less and flicker-free operation. By directly controlling the switching current, the following improvements are made with the proposed LED driver over previous three-port LED drivers. First, the imbalanced energy in a half line cycle experiences one less power conversion step, which reduces conversion loss and improves the overall efficiency. Second, the maximum energy that needs to stored in the transformer in the proposed design is half the amount of conventional and other electrolytic capacitor-less designs, which allows the use of a smaller magnetic core. Third, primary-side current reguation can be easiliy implemented, which can reduce design complexity on the controller circuit. A potential integrated primary-side controller can be implemented based on this method. A 15-W experimental prototype had been built and tested to verify the operating principle. A power factor of 0.94 has been achieved, and each order of harmonic currents is measured, and they are all below the limit from IEC-61000-3-2. The efficiency of the proposed LED driver is only 1.9% lower than a conventional single-stage LED driver at full load, which is a low price to pay when achieving flicker-free operation and electrolytic capacitor-less design. Two 3.3-μF film capacitors have been used in the prototype to buffer double-line-frequency imbalanced energy. The 120-Hz ripple current is measured to be 6% of the average LED current. Overall, the experimental result demonstrates a very good LED driving performance compared with existing options and a high degree of agreement with the analysis presented.

TABLE IV
LOSS BREAKDOWN OF THE PROPOSED CYCLE-BY-CYCLE ENERGY BUFFERING LED DRIVER

	Calculation formula	Result (mW)	Parameters
P_{Q1_cond}	$P_{Q1\_cond}=I_{Q1\_rms}^2\times R_{Q\_on}$	134	P_{Q1_cond}: Conduction loss of Q_1 I_{Q1_rms}: RMS current in Q_1 0.32A
P_{Q1_cap1}	$P_{Q1\_cap1}=\frac{1}{4}C_{Q1\_oss}\times V_{Q1\_ds\_on1}^2\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_on1}=(V_{in\_rec})_{avg}$ when $P_{in}<P_{LED}$	~0	P_{Q1_cap1}: Output capacitor switching loss of Q_1 when $P_{in}<P_{LED}$ $V_{Q1\_ds\_on1}$: Drain to source voltage of Q_1 before turn on when $P_{in}<P_{LED}$ ~60V (average)
P_{Q1_off1}	$P_{Q1\_off1}=\frac{1}{2}\times V_{Q\_ds\_off1}\times I_{Q1\_pk1}\times T_{Q\_f}\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_off1}=V_{sto\_avg}+\frac{N_{pri}}{N_{sec}}\times V_{LED}$	20.6	P_{Q1_off1}: Q_1 turn off switching loss of when $P_{in}<P_{LED}$ I_{Q1_pk1}: Peak switching current in Q_1 when $P_{in}<P_{LED}$ 1A $V_{Q1\_ds\_off1}$: Drain to source voltage of Q_1 after turning off when $P_{in}<P_{LED}$ ~320V
P_{Q1_cap2}	$P_{Q1\_cap1}=\frac{1}{4}C_{Q1\_oss}V_{Q1\_ds\_on2}^2\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_on1}=(V_{in\_rec})_{avg}$ when $P_{in}>P_{LED}$	~0	$V_{Q1\_ds\_on1}$: Drain to source voltage of Q_1 before turn on when $P_{in}>P_{LED}$ ~130V
P_{Q1_off2}	$P_{Q1\_off2}=\frac{1}{2}\times V_{Q\_ds2}\times I_{Q\_pk2}\times T_{Q\_f}\times f_{sw}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$ $V_{Q_1\_ds\_off2}=V_{in\_rec\_avg}+\frac{N_{pri}}{N_{sec}}\times V_{LED}$	6.1	P_{Q1_off2}: 1st turn off overlap switching loss of Q_1 when $P_{in}>P_{LED}$ $V_{Q1\_ds\_off2}$: Drain to source voltage of Q_1 after turn off when $P_{in}>P_{LED}$ ~280V I_{Q1_pk2}: 1st peak switching current in Q_1 when $P_{in}>P_{LED}$ 1A
P_{Q1_off3}	$P_{Q1\_off3}=\frac{1}{2}\times V_{Q\_ds\_off2}\times I_{Q\_pk3}\times T_{Q\_f}\times f_{sw}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$	4.3	P_{Q1_off3}: 2nd turn off overlap switching loss of Q_1 when $P_{in}>P_{LED}$ I_{Q1_pk3}: 2nd peak switching current in Q_1 when $P_{in}>P_{LED}$ 0.5A (the peak switching current changes from 0A to 1A)
P_{D1_cond}	$P_{D_1\_cond}=I_{D_1\_avg}\times V_{D\_F}$	375	P_{D1_cond}: D_1 conduction loss I_{D1_avg}: Average current in D_1 0.25A
P_{Q2_cond}	$P_{Q_2\_cond}=R_{Q\_on}\times I_{Q_2\_rms}^2$	30	P_{Q2_cond}: Conduction loss of D_2 I_{Q2_rms}: RMS current in Q_2 0.15A
P_{D2_cond}	$P_{D_2\_cond}=I_{D_2\_avg}\times V_{D\_F}$	55	P_{D2_cond}: Q_2 conduction loss I_{D2_avg}: RMS current in Q_2 0.04A
P_{Q3_on}	$P_{Q_3\_on}=\frac{1}{2}\times V_{Q_3\_ds\_on}\times I_{Q_3\_pk}\times t_{Q\_r}\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q_3\_ds\_on}=(V_{sto}-V_{in\_rec})_{avg}$	8.8	P_{Q3_on}: Turn on overlap switching loss with Q_3 $V_{Q3\_ds\_on}$: Drain to source voltage of Q_3 before turn on ~70V I_{Q3_pk}: Peak switching current in Q_3 0.17A
P_{Q3_cond}	$P_{Q_3\_cond}=R_{Q\_on}\times I_{Q_3\_rms}^2$	39	P_{D3_cond}: Conduction loss of D_3 I_{Q3_rms}: RMS current in Q_3 0.16A
P_{D3_cond}	$P_{D_3\_cond}=I_{D_3\_avg}\times V_{D\_F}$	52	P_{D3_cond}: Conduction loss of D_3 I_{D3_avg}: RMS current in Q_3 0.04A
P_{Q3_cap}	$P_{Q1\_cap}=\frac{1}{4}C_{Q\_oss}\times V_{Q_3\_ds\_on}^2\times f_{sw}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$	0.3	P_{Q3_cap}: Q_3 output capacitor switching loss
P_{lk1}	$P_{lk1}=\frac{1}{2}I_{Q_1\_pk2}^2\times L_{lk1\_est}\times\frac{2T_{P_{in}<P_{LED}}}{T_{line}}$	300	P_{lk1}: Leakage inductor loss when $P_{in}<P_{LED}$ L_{lk1_est}: Estimated leakage inductance between the primary side main winding and the second side main winding 4% x L_{pri} = 48μF
P_{lk2}	$P_{lk2}=\frac{1}{2}I_{Q\_pk2}^2\times L_{lk1}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$	300	P_{lk2}: Leakage inductor loss generated by the first primary pulse current when $P_{in}<P_{LED}$
P_{lk3}	$P_{lk3}=\frac{1}{2}I_{Q\_pk3}^2\times L_{lk2}\times\frac{2T_{P_{in}>P_{LED}}}{T_{line}}$	75	P_{lk3}: Leakage inductor loss generated by the second primary pulse current when $P_{in}<P_{LED}$ L_{lk2}: Leakage inductance between the primary side main winding and the buffer winding 24μF
P_{tran_est}	$P_{tran}=P_{LED}\times(1+\frac{1}{\pi})\times 2\%$	395	P_{tran_est}: Estimated sum of core and copper losses of the Flyback transformer 2% P_{LED} = 0.3W
Total		1815	

APPENDIX

For the MOSFET, the following parameters are used in the loss calculation:

C_{Q_oss}: MOSFET parasitic output capacitance 13 pF;
R_{Q_on}: ON resistance of the MOSFET 1.4 Ω;
T_{Q_f}: MOSFET Turn-OFF fall time 15 ns;
T_{Q_r}: MOSFET turn-ON rise time 15 ns;

For the diode, the following parameter is used in the loss calculation:

V_{D_F}: Diode forward voltage drop 1.5 V.

The switching frequency is 25 kHz. The loss breakdown of the proposed cycle-by-cycle enregy buffering LED driver and the previous active filtering LED driver is shown in Tables IV and V, respectively.

TABLE V
LOSS BREAKDOWN OF THE PREVIOUS ACTIVE FILTERING LED DRIVER

	Calculation formula	Result (mW)	Parameters
P_{Q1_cond}	$P_{Q1\_cond} = I_{Q\_rms}^2 \times R_{Q\_on}$	134	P_{Q1_cond} : Conduction loss of Q_1 I_{Q1_rms} : RMS current in Q_1 0.3A
P_{Q1_cap}	$P_{Q1\_cap} = \frac{1}{4} C_{Q\_oss} V_{Q1\_ds\_on}^2 \times f_{sw} \times \frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q1\_ds\_on} = (V_{in\_rec})_{avg}$	1	P_{Q1_cap1} : Output capacitor switching loss of Q_1 $V_{Q1\_ds\_on}$: Drain to source voltage of Q_1 before turn on ~100V
P_{Q1_off}	$P_{Q1\_off} = \frac{1}{2} \times V_{Q1\_ds\_off} \times I_{Q1\_pk} \times T_{Q\_f} \times f_{sw} \times \frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Q1\_ds\_off} = (V_{in\_rec})_{avg} + \frac{N_{pri}}{N_{sec}} \times V_{LED}$	13	P_{Q1_off} : Q_1 turn off switching loss of I_{Q1_pk} : Peak switching current in Q_1 1A (rms) $V_{Q1\_ds\_off}$: Drain to source voltage of Q_1 after turn off ~280V
P_{D1_cond}	$P_{D1\_cond} = I_{D1\_avg} \times V_{D1\_F}$	375	P_{D1_cond} : D_1 conduction loss I_{D1_avg} : Average current in D_1 0.25A
P_{lk}	$P_{Q1\_cond} = \frac{1}{2} I_{Q1\_pk}^2 \times L_{lk} \times \frac{2T_{P_{in}<P_{LED}}}{T_{line}}$	600	P_{lk} : Leakage inductor loss L_{lk_est} : Estimated leakage inductance between the primary side main winding and the second side main winding 4% x L_{pri} = 48μF
P_{tran}	$P_{tran} = P_{LED} \times 2\%$	300	P_{tran_est} : Estimated sum of core and copper losses of the Flyback transformer 2% P_{LED} = 0.3W
P_{QBuck_cond}	$P_{Q_{Buck}\_cond} = I_{Q_{Buck}\_rms}^2 \times R_{Q\_on}$	49	P_{QBuck_cond} : MOSFET conduction loss in the Buck converter I_{QBuck_rms} : RMS current in the MOSFET of the Buck converter 0.187A
P_{QBuck_off}	$P_{Q1\_off} = \frac{1}{2} \times V_{QBuck\_ds\_off} \times I_{QBuck\_pk} \times T_{Q\_f} \times f_{sw} \times \frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{QBuck\_ds\_off} = (V_{sto})_{avg}$	7.7	P_{QBuck_off} : MOSFET switching loss in the Buck converter I_{QBuck_pk} : Peak current in the MOSFET 0.59A $V_{QBuck\_ds\_off}$: Drain to source voltage across the MOSFET before turn off ~140V
P_{QBuck_cap}	$P_{Q1\_cap} = \frac{1}{2} \times C_{Q\_oss} V_{Qbuck\_ds\_on}^2 \times f_{sw} \times \frac{2T_{P_{in}<P_{LED}}}{T_{line}}$ $V_{Qbuck\_ds\_on} = (V_{sto})_{avg} - V_{LED}$	1.6	P_{QBuck_cap} : MOSFET output capacitor switching loss in the Buck converter $V_{QBuck\_ds\_on}$: Drain to source voltage across the MOSFET before turn on ~80V
P_{Dbuck_cond}	$P_{DBuck\_cond} = I_{D_{Buck}\_avg} \times V_{D\_F}$	138	P_{DBuck_cond} : Diode conduction loss in the Buck converter I_{DBuck_avg} : Average current in the diode 0.09A
$P_{inductor\_Buck}$	$P_{inductor\_Buck} = P_{Buck} \times 2\%$	95.5	P_{Buck} : Buck converter output power $P_{inductor\_Buck}$: Estimated loss of inductor in the Buck converter 2% x P_{Buck}
P_{Qboost_cond}	$P_{Q_{Boost}\_cond} = I_{Q_{Boost}\_rms}^2 \times R_{Q\_on}$	51.6	P_{QBoost_cond} : MOSFET conduction loss in the Boost converter I_{QBoost_rms} : RMS current in the MOSFET of the Boost converter 0.192A
P_{Qboost_off}	$P_{QBoost\_off} = \frac{1}{2} \times V_{QBoost\_ds\_off} \times I_{QBoost\_pk} \times T_{Q\_f} \times f_{sw} \times \frac{2T_{P_{in}>P_{LED}}}{T_{line}}$ $V_{QBoost\_ds\_off} = V_{LED}$	3.3	P_{QBoost_off} : MOSFET switching loss in the Boost converter I_{QBoost_pk} : Peak current in the MOSFET 0.59A $V_{QBoost\_ds\_off}$: Drain to source voltage across the MOSFET after turn off 60V
P_{Qboost_cap}	$P_{Q1\_cap} = \frac{1}{2} C_{QBoost\_oss} \times V_{QBoost\_ds\_on}^2 \times f_{sw} \times \frac{2T_{P_{in}>P_{LED}}}{T_{line}}$ $V_{QBoost\_ds\_on} = (V_{sto})_{avg}$	0.3	P_{QBoost_cap} : MOSFET output capacitor switching loss in the Boost converter $V_{QBuck\_ds\_on}$: Drain to source voltage across the MOSFET before turn on ~140V
P_{DBoost_cond}	$P_{DBoost\_cond} = I_{D_{Boost}\_avg} \times V_{D\_F}$	102	P_{QBoost_cond} : MOSFET output capacitor switching loss in the Boost converter I_{DBoost_avg} : Average current in the diode 0.068A
$P_{inductor\_Boost}$	$P_{Inductor\_Boost} = P_{Boost} \times 2\%$	95.5	P_{Boost} : Boost converter output power $P_{inductor\_Boost}$: Estimated loss of inductor in the Boost converter 2% x P_{Boost}
Total		2006	

REFERENCES

[1] ENERGY STAR Program Requirements for Solid State Lighting Luminaires, Version 1.1, Dec. 19, 2008.

[2] *Electromagnetic Compatibility (EMC), in Part 3: Limits—Section II: Limits for Harmonic Current Emissions (Equipment Input Current < 16 A, per Phase)*, Standard IEC61000-3-2, 1991.

[3] B. Lehman and A. J. Wilkins, "Designing to mitigate effects of flicker in LED lighting: Reducing risks to health and safety," *IEEE Power Electron. Mag.*, vol. 1, no. 3, pp. 18–26, Sep. 2014.

[4] B. Lehman, A. Wilkins, S. Berman, M. Poplawski, and N. J. Miller, "Proposing measures of flicker in the low frequencies for lighting applications," in *Proc. Energy Convers. Congr. Expo.*, Phoenix, AZ, USA, Sep. 2011, pp. 2865–2872.

[5] *IEEE Recommended Practices for Modulating Current in High-Brightness LEDs for Mitigating Health Risks to Viewers*, IEEE Standard 1789-2015, Jun. 5, 2015.

[6] X. B. Ruan, B. B. Wang, K. Yao, and S. Wang, "Optimum injected current harmonics to minimize peak-to-average ratio of LED current for electrolytic capacitor less AC–DC drivers" *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1820–1825, Jul. 2011.

[7] G. G. Pereira, M. A. Dalla Costa, J. M. Alonso, M. F. De Melo, and C. H. Barriquello, "LED driver based on input current shaper without electrolytic capacitor," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4520–4529, Jun. 2017.

[8] D. G. Lamar, J. Sebastian, M. Arias, and A. Fernandez, "On the limit of the output capacitor reduction in power-factor correctors by distorting the line input current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1168–1176, Mar. 2012.

[9] F. H. Zhang, J. J. Ni, and Y. J. Yu, "High power factor AC–DC LED driver with film capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4831–4840, Oct. 2013.
[10] C. A. Cheng, C. H. Chang, T. Y. Chung, and F. L. Yang, "Design and implementation of a single-stage driver for supplying an LED street-lighting module with power factor corrections," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 956–966, Feb. 2015.
[11] J. C. W. Lam and P. K. Jain, "Isolated AC/DC offline high power factor single-switch LED drivers without electrolytic capacitors," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 3, pp. 679–690, Sep. 2015.
[12] J. C. W. Lam and P. K. Jain, "A high power factor, electrolytic capacitorless AC-input LED driver topology with high frequency pulsating output current," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 943–955, Feb. 2015.
[13] H. Ma, J. S. Lai, C. Zheng, and P. Sun, "A high-efficiency quasi-single-stage bridgeless electrolytic capacitor-free high-power AC–DC driver for supplying multiple LED strings in parallel," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5825–5836, Aug. 2016.
[14] P. Fang, Y. F. Liu, and P. C. Sen, "A flicker-free single-stage offline LED driver with high power factor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 3, pp. 654–665, Sep. 2015.
[15] P. Fang, Y. j. Qiu, H. Wang, and Y. F. Liu, "A single-stage primary-side-controlled off-line flyback LED driver with ripple cancellation," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4700–4715, Jun. 2017.
[16] P. Fang and Y. F. Liu, "Energy channeling LED driver technology to achieve flicker-free operation with true single stage power factor correction," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3892–3907, May 2017.
[17] Y. Qiu, L. Wang, H. Wang, Y. F. Liu, and P. C. Sen, "Bipolar ripple cancellation method to achieve single-stage electrolytic-capacitor-less high-power LED driver," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 3, pp. 698–713, Sep. 2015.
[18] D. Camponogara, G. F. Ferreira, A. Campos, M. A. Dalla Costa, and J. Garcia, "Offline LED driver for street lighting with an optimized cascade structure," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2437–2443, Dec. 2013.
[19] E. Rifa, *Electrolytic Capacitors Application Guide, Appl. Note*, Evox Rifa AB, Gränna, Sweden, 2001.
[20] Q. C. Hu and R. Zane, "Minimizing required energy storage in off-line LED drivers based on series-input converter modules," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2887–2895, Oct. 2011.
[21] S. Wang, X. B. Ruan, K. Yao, S. C. Tan, Y. Yang, and Z. H. Ye, "A flicker-free electrolytic capacitor-less AC–DC LED driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4540–4548, Nov. 2012.
[22] G. C. Christidis, A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "Investigation of parallel active filters' limitations for power decoupling on single-stage/single-phase microinverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1096–1106, Sep. 2016.
[23] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.
[24] M. Hadi Zare, M. Mohamadian, and R. Beiranvand, "A single-phase grid-connected photovoltaic inverter based on a three-switch three-port flyback with series power decoupling circuit," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2062–2071, Mar. 2017.
[25] C. Y. Liao, W. S. Lin, Y. M. Chen, and C. Y. Chou, "A PV microinverter with PV current decoupling strategy," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6544–6557, Aug. 2017.
[26] H. Hu, S. Harb, N. H. Kutkut, Z. J. Shen, and I. Batarseh, "A single-stage microinverter without using electrolytic capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2677–2687, Jun. 2013.
[27] W. Chen and S. Y. R. Hui, "Elimination of an electrolytic capacitor in AC/DC light-emitting diode (LED) driver with high input power factor and constant output current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1598–1607, Mar. 2012.
[28] Y. C. Li and C. L. Chen, "A novel primary-side regulation scheme for single-stage high-power-factor AC–DC LED driving circuit," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4978–4986, Nov. 2013.
[29] X. G. Xie, J. Wang, C. Zhao, Q. Lu, and S. R. Liu, "A novel output current estimation and regulation circuit for primary side controlled high power factor single-stage flyback LED driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4602–4612, Nov. 2012.
[30] *14 W TRIAC Dimmable, High Efficiency >85%, Non-Isolated Buck Converter, Power Factor Corrected (>0.95) LED Driver Using LYTSwitchTM LYT4313E*, Power Integration, San Jose, CA, USA, 2013.
[31] *AN-2150 LM3450A Evaluation Board*, Texas Instruments, Dallas, TX, USA, 2013.

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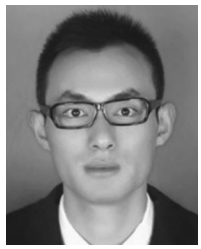

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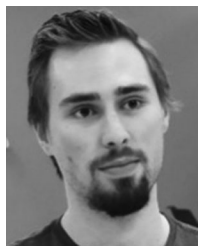

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